## REMARKS/ARGUMENTS

Claims 1-23 remain in this application.

### 1. Objection to the Drawings

FIGS. 10 & 11 stand objected to under 37 CFR 1.83(a) for not showing "delay element 1004" (p. 15, line 24) and "logic element 1104" (p. 15, line 27).

In response to the Examiner's objection, applicant reviewed FIGS. 10 & 11 and found element 1004 in about the middle of FIG. 10, and element 1104 in about the middle of FIG. 11. Thus, no correction for these omissions is believed to be necessary. Applicant does note, however, that a line connecting element 1102, element 1104, and an input of element 812 is missing in FIG. 11. An amendment to FIG. 11 to add this line has therefore been made. It is believed that the addition of this line does not introduce new matter, as a similar line is shown in FIG. 10, and it is believed that one of ordinary skill in the art would readily recognize that this line was missing.

### 2. Rejection of Claims 1, 9 and 14 Under 35 USC 112, 2nd Paragraph

Claims 1, 9 and 14 stand rejected under 35 USC 112, 2nd Paragraph, as being indefinite in that they use the phrase "may be".

The phrase "may be" has been changed to "is" in each of these claims. It is believed that this change maintains the scope of the originally filed claims and, thus, does not introduce new matter.

3. Rejection of Claims 1-20 Under 35 USC 103(a)

Claims 1-20 stand rejected under 35 USC 103(a) as being unpatentable over Wagner et al. (U.S. Pat. No. 6,389,566; hereinafter "Wagner").

In rejecting applicant's claim 1, the Examiner asserts that Wagner teaches a serial scan chain, but does not explicitly teach "current surge minimization circuitry which is interconnected with [a] plurality of interconnected circuit elements, whereby operation of said current surge minimization circuitry during operation of [a] number of scan chains minimizes current surges in [an] integrated circuit." Applicant agrees with the Examiner on this point.

The Examiner also asserts that Wagner teaches:

> . . .scan shift race conditions are minimized by providing a weak scan output signal driver and inserting delay elements within a cell for a scan flip-flop in the scan signal path (abstract, col. 3, lines 39-58) and further Wagner et al. teach a preceding equation for avoiding race conditions during scan shift operations (see col. 6, lines 15-30) including applying the functionality of CMOS device ***(In CMOS technology, both kinds of transistors (N-type transistors) or (P-type transistors) are used in a complementary way to form a current gate that forms an effective means of electrical control and as the current direction changes more rapidly, however, the transistors become hot. This characteristic tends to limit the speed at which microprocessors can operate)*** for minimizing the race ***(surge)*** current ***(see col. 6, lines 31-45)*** which Wagner's system is basically teaching the same system and method as the applicant's claim to minimize current.
>
> 3/11/04 Office Action, sec. 4, pp. 3-4 (emphasis added).

Applicant respectfully disagrees. The Examiner seems to suggest, although perhaps inadvertently, that the emphasized portions of his assertions are taught or suggested by Wagner in col. 6, lines 31-45. This is absolutely not the case. In fact, Wagner's entire disclosure is void of any discussion of "transistors becoming hot" or currents "surging". Rather, Wagner's race mitigation techniques are designed to prevent "an incorrect test vector being loaded into the scan chain or an inaccurate reading of the system state being provided." See Wagner, col. 3, lines 13-14.

Although the Examiner suggests that one of ordinary skill in the art would think to modify Wagner's teachings for the purpose of minimizing current surges during scan chain operation, applicant does not believe this to be the case. Of note, Wagner discloses the incorporation of delay elements in the path along which test data is shifted (i.e., from $S_{IN}$ to $S_{OUT}$; see, e.g., Wagner's FIG. 2). Although Wagner's delay elements might help to mitigate *race conditions* in the scan chain's data path, applicant fails to see how Wagner's delay elements would minimize *current surges*. The addition of more active transistors in the scan chain's data path would seem to only increase the current draw of the scan chain (and not minimize current surges).

For the above reason, applicant believes the Examiner's rejection of his claim 1 is not supported, and should be withdrawn. Applicant's claims 2-8 are believed to be allowable at least for the reason that they depend from claim 1. However, applicant's claims 2-8 are also believed to be allowable for other reasons, some of which are discussed below.

With respect to applicant's claim 2, the Examiner discusses how Wagner teaches how to avoid race conditions "by increasing the signal transition time of a flip-flop during a shift operation" and by using a weak signal driver that has low current drive capability. See 3/11/04 Office Action, sec. 4, p. 4. However, applicant fails to see the relation of this teaching to his claim. His claim discloses the use of "transistors receiv[ing] a number of gating signals during operation of [a] number of scan chains, which number of gating signals disable current flow through the ones of said plurality of interconnected circuit elements." Although Wagner does disclose the use of gating signals, Wagner's gating signals are in a scan chain's data path, and they do not readily appear to mitigate current surges in "circuit elements" that are "interconnected with" a "number of scan chains".

With respect to applicant's claim 3, the Examiner does not disclose where Wagner teaches "an electrical network connecting gates of the number of [gated] transistors to one or more external inputs of the integrated circuit".

With respect to applicant's claim 4, the Examiner does not disclose where Wagner teaches "a number of delay elements which cause a signal applied to one of

said external inputs to be applied to the gates of various of said number of [gated] transistors at different times".

With respect to applicant's claim 5, the Examiner does not disclose where Wagner teaches "a number of logic elements which cause at least one of said number of gating signals to change state in response to data shifted through at least one of said number of scan chains".

With respect to applicant's claim 6, the Examiner asserts that Wagner teaches the elements of this claim in col. 1, last paragraph. However, this paragraph does not teach "at least first and second scan chains" or "external shift signal inputs corresponding to the first and second scan chains". In fact, applicant cannot find such teachings anywhere in Wagner's disclosure.

As with claim 6, applicant's claim 7 recites "first and second scan chains", which feature does not appear to be taught anywhere in Wagner's disclosure.

Applicant's claims 9-11 are believed to be allowable at least for reasons similar to why applicant's claim 1 is believed to be allowable. Applicant's claim 11 is also believed to be allowable in that Wagner does not teach phased operation of at least two scan chains. Although the Examiner asserts that such phased operation is commonly known to those of ordinary skill in the art, applicant requests that the Examiner provide a reference to support this assertion. However, if the Examiner allows applicant's claim 11 as a result of its dependence on claim 9, such a reference need not be produced.

Applicant's claim 12 has been amended, and support for its amendment is found, at least, in applicant's original claim 1. Thus, it is believed that applicant's amendment to claim 12 does not introduce new matter. With this amendment, it is believed that applicant's claims 12 and 13 are allowable at least for reasons similar to why applicant's claim 1 is believed to be allowable.

Applicant's claim 14 has been amended, and support for its amendment is found, at least, in applicant's original claim 1. Thus, it is believed that applicant's amendment to claim 14 does not introduce new matter. With this amendment, it is believed that applicant's claims 14-17 are allowable at least for reasons similar to why applicant's claim 1 and other claims are believed to be allowable.

Applicant's claims 18-20 are believed to be allowable at least for reasons similar to why applicant's claim 1 and other claims are believed to be allowable.

## 4. Rejection of Claims 21-23 Under 35 USC 103(a)

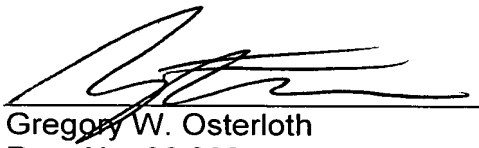
Claims 21-23 stand rejected under 35 USC 103(a) as being unpatentable over Wu (U.S. Pat. No. 5,831,992).

In rejecting applicant's claims 21-23, the Examiner cites a reference (Wu) that discloses the use of two scan chains. However, the Examiner then admits that the remaining limitations of applicant's claims (e.g., out-of-phase operation of the two scan chains) are not actually taught by Wu, but would be obvious to one of ordinary skill in the art. However, similarly to applicant's response to the Examiner's rejection of his claim 11, applicant requests that the Examiner provide a reference to support this assertion. In the absence of such a reference, applicant believes his claims 21-23 to be allowable.

## 5. Conclusion

In light of the amendments and remarks provided herein, applicant respectfully requests the timely issuance of a Notice of Allowance.

Respectfully submitted,
DAHL & OSTERLOTH, L.L.P.

By: 

Gregory W. Osterloth
Reg. No. 36,232
Tel: (303) 291-3200

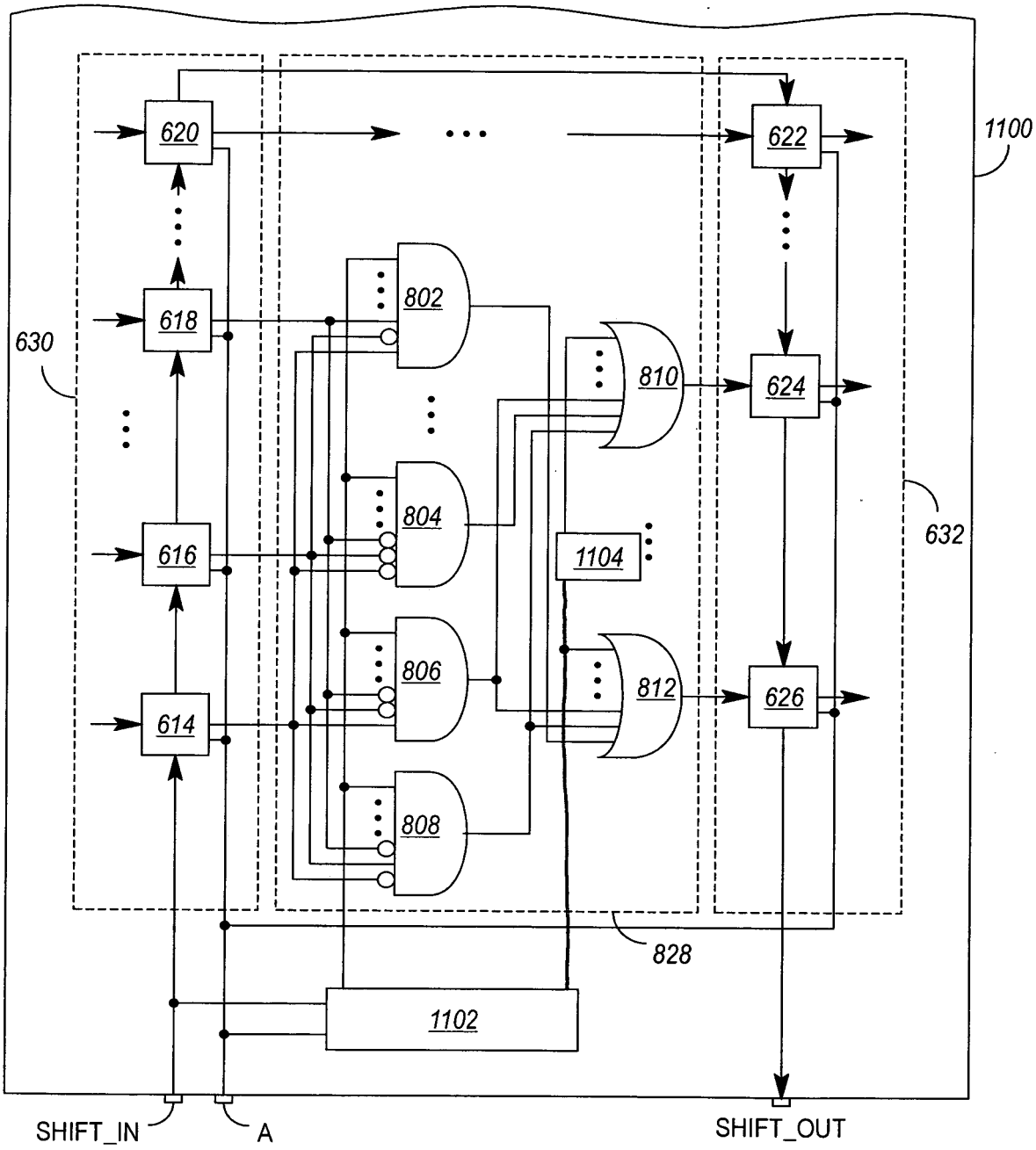



FIG. 11